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TITLE: TEST MODE SETUP CIRCUIT FOR MICROCONTROLLER UNIT

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TEST MODE SETUP CIRCUIT FOR MICROCONTROLLER UNIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device, and in particular, to a test circuit for a microcontroller unit (MCU).

2. Background of the Related Art

Fig. 1 is a schematic block diagram that illustrates a related art test mode setup circuit for a microcontroller unit (MCU). The related art test mode setup circuit is composed of a test pin 10.1 for receiving a test signal, a reset pin 10.2 for receiving a reset signal, a clock pin 10.3 for receiving a clock signal CLK and a test mode related circuit 10 for outputting a test mode related signal to an internal circuit when receiving the test signal over the test pin 10.1. The clock signal CLK is preferably generated using an oscillator (not shown).

In a normal mode, the test mode related circuit 10 is not connected with an internal circuit of the MCU. After a test mode is established, that is when a test signal inputted over the test pin 10.1 becomes active, the test mode related circuit 10 outputs the test mode related signal to the internal circuit to place the internal circuit in the test mode.

However, a MCU having a small number of pins has been produced in large numbers. Accordingly, as described above, the related art test mode setup circuit has various disadvantages. When the test pin is added to the MCU having the small number of pins in addition to essentially required pins such as the reset pin, a VDD pin, a VSS pin and a clock pin, a number of pins that are available for a user is decreased. Further, since the test pin is a pin that the user does not generally use (i.e., in normal operations), usability and applicability of the MCU is deteriorated.

The above references are incorporated by reference herein where appropriate for appropriate teachings of additional or alternative details, features and/or technical background.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a test circuit for a MCU that substantially obviates one or more of the problems caused by limitations and disadvantages of the related art.

Another object of the present invention is to provide a test mode setup circuit for a MCU having a small number of pins.

Another object of the present invention is to provide a test circuit for a MCU that sets a test mode without adding a separate test pin.

Another object of the present invention is to provide a test mode setup circuit for a MCU that sets a test mode using only a reset pin and a clock pin.

To achieve at least the above-identified objects in a whole or in parts there is provided a test circuit for a microcontroller according to the present invention that includes a first pin receiving a first signal; a second pin receiving a second signal; and a test signal generating circuit that generates a test signal in response to a logical combination of the first signal and the second signal.

To further achieve at least the above-described objects in a whole or in parts there is provided a microcontroller unit according to the present invention that includes a clock pin that receives a clock signal; a reset pin that receives a reset signal; a test mode counter that is set and reset based on the clock signal and the reset signal to count the reset signal; and a decoder that activates a test mode flag when a count value of the test mode counter reaches a prescribed value.

To further achieve at least the above-described objects in a whole or in parts there is provided a test mode setup circuit for a microcontroller unit according to the present invention that includes a clock pin that receives a clock signal; a reset pin that receives a reset signal; a test signal generating circuit that counts the reset signal in accordance with a combination of the clock signal and the reset signal to generate a test signal, wherein the test signal generating circuit includes, a logic gate that logically processes the clock signal

and the reset signal, a test mode counter that is set and reset in accordance with an output signal from the logic gate to count the reset signal, and a decoder that outputs the test signal when a count value from the test mode counter is a prescribed count value; and a test mode related circuit operated by the clock signal and the reset signal that enters an internal circuit into a test mode in accordance with the test signal from the test signal generating circuit.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objects and advantages of the invention may be realized and attained as particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements, and wherein:

Fig. 1 is a block diagram of a related art test mode setup circuit for an MCU;

Fig. 2 is a block diagram of a preferred embodiment of a test circuit for an MCU according to the present invention; and

Figs. 3A through 3D are diagrams showing input and output timing waveforms of elements in Fig. 2.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Fig. 2 is a schematic block diagram showing a preferred embodiment of a test mode setup circuit according to the present invention. As shown in Fig. 2, the test mode setup circuit for a microcontroller unit (MCU) or the like preferably includes an OR gate 20, a test mode counter 30 and a decoder 40. The preferred embodiment of the test mode setup circuit further includes a test mode related circuit 10, and only includes a clock pin 10.3 and a reset pin 10.2 as input pins.

The OR gate 20 ORs a clock signal CLK that is inputted to the clock pin 10.3, and a reset signal RESET that is inputted to the reset pin 10.2. The OR gate 20 transmits an output signal to a reset terminal RSTb of the test mode counter 30.

The test mode counter 30 is preferably set or reset in accordance with the output signal from the OR gate 20 received via the reset terminal RSTb and preferably counts the reset signal RESET that is inputted over the reset pin 10.2. The test mode counter 30 is preferably reset by a low-level signal. However, the present invention is not intended to be so limited.

The decoder 40 receives a test count value from the test mode counter 30 and activates a test mode flag when the input count value becomes a prescribed test mode count value. The test mode related circuit 10 outputs a test mode related signal to the internal circuit (not shown) in accordance with the active test mode flag from the decoder 40.

Operations of the preferred embodiment of the test mode setup circuit for the MCU of the present invention will now be described. In a normal mode, the internal circuit (not shown) is synchronized for operations by the clock signal CLK, which is inputted using the clock pin 10.3.

In a test mode, when the clock signal CLK, which is inputted using the clock pin 10.3, becomes a high level as shown in Fig. 3A, the operation of the internal circuit is suspended, and the test mode counter 30 is set by a high-level signal outputted from the OR gate 20. Accordingly, the test mode counter 30 receives the reset signal RESET, as shown in Fig. 3B, which is preferably input to a clock terminal over the reset pin 10.2. The test mode counter 30 preferably counts a rising edge or a falling edge of the reset signal to output a count value as shown in Fig. 3C. The decoder 40 receives the count value from the test mode counter 30 and activates the test mode flag when the input count value from the test mode counter 30 is a predescribed test mode count value.

For example, assume that the test mode count value that has been previously set up in the decoder 40 is hexidecimal FF. The decoder 40 disables the test mode flag when receiving any other count values (ϕ0, ϕ1, ϕ2, ϕ3,..., FD, FE) from the test mode counter 30 and enables the test mode flag when the count value FF is received from the test mode counter 30.

Accordingly, the test mode related circuit 10 outputs a test mode related signal to the internal circuit (not shown) in accordance with the enabled test mode flag to enter the internal circuit into the test mode. As shown in Figs. 3A-3D, the internal circuit preferably enters the test mode from the time (t).

In addition, with the preferred embodiment of the present invention, it becomes possible to set up a test mode count value of the test mode counter 30 in various ways and to achieve various test modes by decoding various test mode count values.

As described above, the preferred embodiment of the test mode setup circuit for the MCU according to the present invention has various advantages. The test mode setup circuit sets up the test mode using only the reset pin and the clock pin without having a separate test pin. Thus, the preferred embodiment of a test mode setup circuit for a MCU or the like can be used for the MCU having a reduced or small number of pins. Further, various test modes can be achieved by which the test mode count value of the test mode counter is decoded in different ways.

The foregoing embodiments are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures.